UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,370	07/07/2005	Hans-Detlef Groeger	P05,0091	6471

26574 7590 05/21/2008

SCHIFF HARDIN, LLP
PATENT DEPARTMENT
6600 SEARS TOWER
CHICAGO, IL 60606-6473

EXAMINER	
PHAM, HAI CHI	
ART UNIT	PAPER NUMBER
2861	

MAIL DATE	DELIVERY MODE
05/21/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,370	GROEGER, HANS-DETLEF	
	Examiner	Art Unit	
	Hai C. Pham	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

- Page 8, line 21, "an input interface 50" should read --an input interface 48--;
- Page 8, line 23, "an output interface" should read --an output interface 50--.

Appropriate correction is required.

Claim Objections

2. Claims 33, 35, 36 and 41 are objected to because of the following informalities:

Claim 33:

- Line 2, "is reproduces" should read --is reproduced--.

Claim 35:

- The following limitation "as said memory in the functional unit volatile memory is provided in which said data are stored" should read -- ~~as~~ said memory in the functional unit being volatile memory ~~is provided~~ in which said data are stored--.

Claim 36:

- Line 2, "late" should read --light--.

Claim 41:

- The following limitation "as said memory data are stored in a volatile memory that is separately assigned of the functional unit" should read -- ~~as~~ said memory

is a volatile memory and said memory data are stored in said volatile memory that is separately assigned of the functional unit --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 33, 38-43 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 33:

- The following limitation "the functional units have a system clock" appears to be ambiguous in that it indicates that the system clock is internal to the functional units. It is suggested to reword the claim limitation as follows --the functional units receive the clock signal from a system clock by which the input clock signal is reproduced--.

Claim 38:

- The following limitation "and a temporal beginning of the illumination phases of groups of light sources being selectable by use of the functional unit which ... are minimized" is not a structural limitation that further defines the apparatus claim 38. It is suggested to amend the claim limitation as follows --wherein the

functional unit selects a temporal beginning of the illumination phases of groups of light sources, and wherein the functional unit receives ... are minimized--.

Claim 39:

- The following limitation "the functional units have a system clock" appears to be ambiguous in that it indicates that the system clock is internal to the functional units. It is suggested to reword the claim limitation as follows --the functional units receive the clock signal from a system clock by which the input clock signal is reproduced--.

Claim 45:

- The following limitation "and a temporal beginning of the illumination phases of groups of light sources being selectable by use of the functional unit which receives ... are minimized" is not a structural limitation that further defines the apparatus claim 38. It is suggested to amend the claim limitation as follows -- wherein the functional unit selects a temporal beginning of the illumination phases of groups of light sources, and wherein the functional unit receives ... are minimized--

Claims 40-43 are dependent from claim 38 above and are therefore indefinite. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 32-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bizen (JP 2002-211042) in view of Soma et al. (JP 3-98084) and Katakura et al. (US 5,892,532).

With regard to claims 38 and 45, Bizen discloses a LED printer comprising a character generator (optical print head having an array of light-emitting elements 1) (Fig. 1) that has a plurality of light sources arranged in at least one row in groups (the light emitting elements are arranged in one row in 26 separate groups) (Fig. 2), a separate functional unit (driving ICa1 through ICa26) for each light source group for controlling of the light sources (the driving ICa1 through ICa26 are dedicated to the respective 26 groups of light emitting elements), the functional unit is connected with a central control unit (control circuit 6 of the printer) (Fig. 2), the functional unit comprising an input (i.e. input terminals LI, CI and SI) via which it can receive data (i.e. input terminal SI for receiving data) and a clock signal (i.e. input terminal CI for receiving the clock signal CLK) and an output (i.e. output terminals LO, CO and SO) via which the functional unit can forward data (i.e. output terminal SO for forwarding data) and a clock signal (i.e. output terminal CO for forwarding the clock signal CLK) to the functional unit that is subsequent in the row except for the last functional unit in the row (i.e. the last functional unit being the driving Ica1) (Fig. 2), a memory (store circuit 13 storing the Y-location amendment data) (Fig. 3), and a control unit (timing control circuit 14) (Fig. 3), said memory of the functional unit having stored therein data targeted by use of said

address to the respective function unit (the device includes a flash memory 5 for storing the data for compensating the location gap in the Y-direction of the light emitting elements of the 26 groups, the data being read from the memory 5 into the individual internal store circuit 13 of the respective driving ICa1-ICa26, the reading from one memory and the writing to another memory require specific address as it is commonly known in the art; in other words, the address is inherently part of the memories and the driving ICs), the light sources of each group being controlled by said control unit assigned to the respective functional unit (each of the driving ICa1-ICa26 has its own timing control circuit 14 for controlling the lighting timing of the light emitting elements in the corresponding group), the at least one light source row being imaged as an exposure line onto the recording medium, which is displaced substantially transverse to the exposure line relative to the character generator (Figs. 7A-7E), and a temporal beginning of the illumination phases of groups of light sources being selectable by use of the functional unit which receives a respective start command from said central control unit and uses said start command within the functional unit to individually initiate said temporal beginning of each said respective group such that deviations of the exposure line from a target line are minimized (the timing control circuit 14 of each of the driving IC receives a timing signal STB from the control circuit 6 to start the lighting timing of the light emitting elements of the group; moreover, the lighting timing is selectively controlled not only for each individual light emitting element but also for different groups of the light emitting elements belonging to different driving ICs so as to

correct for the deviation of the print line with respect to the reference line position) (English translation [0041]-[0042], [0061]-[0070]) (see also Figs. 7A-7E).

Although Bizen discloses the individual driving ICs and the memories being accessed through signal buses on the basis of addresses, Bizen however does not explicitly teach the address decoder being included in the respective functional units, i.e. driving ICs.

Soma et al. discloses in Fig. 1 a light emitting diode lighting circuit comprising a plurality of light emitting diodes (30) arranged in at least one row in groups, a separate functional unit or driving IC 20 for each light emitting group for controlling of the light emitting diodes, wherein each of the driving ICs includes an internal address decoder (21) for decoding an address signal (41) to output a signal indicative of the position of the respective light emitting diodes (30) in the array such that the lighting information signal can be received by the proper light emitting diodes (see Abstract).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the driving ICs of Bizen with the internal address decoders as taught by Soma et al. The motivation for doing so would have been to provide the driving circuitry with an efficient means for controlling and directing the correction data as well as the image data to the proper light emitting elements in the array to reduce the otherwise large external memory writing control.

Bizen also fails to teach the intermediate carrier to carry the image exposed by the light source.

However, it is well known in the art that image can be formed on an intermediate carrier such as the photosensitive drum to be transferred onto the paper or directly to a photosensitive recording medium supported on the drum. Katakura et al. discloses a LED printer comprising an intermediate carrier or photosensitive drum (not shown) and a transferring section for transferring the toner image formed on the photosensitive drum onto paper (col. 3, line 45-54).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the device of Bizen with the photosensitive drum and the image transferring section as taught by Katakura et al. since Katakura et al. teaches this to be well known in the art to formed a latent image on the photosensitive drum to be transferred onto paper.

The method of claims 32 and 44 correspond to the operation of the device of claims 38 and 45, respectively, and the art applied towards claims 38 and 45 are analogously applied towards claims 32 and 44.

Bizen also discloses the driving ICs including internal memory (13) for storing compensation data (Fig. 3), but does not explicitly disclose the memory being volatile memory (claims 35, 41), and the data comprising a correction parameter for each light source of the group that represents its individual illumination intensity (claims 37, 43).

Katakura et al. discloses a LED printer comprising optical print head (35) including a plurality of light emitting elements arranged in a row in plural groups, each group having a separate functional unit or IC chips drivers DRs. Katakura et al. further teaches volatile memories 78a-78d being provided in each functional unit or driver DR

for storing the current values for adjusting the drive current of the respective light-emitting elements of the group so as to reduce the variation in light emitting intensity between each light emitting elements of the group and to prevent change in dot shape (col. 11, lines 3-25).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the device of Bizen with the volatile memories assigned to each functional unit for storing the correction intensity data for each light source of the group as taught by Katakura et al. The motivation for doing so would have been to reduce the variation in light emitting intensity between each light emitting elements of the group and to prevent change in dot shape as suggested by Katakura et al.

Bizen further teaches:

- (regarding claims 33, 39) the functional units have a system clock by which the clock signal is reproduced (the system clock CLOCK fed by the control circuit 6 of the printer to the first driving ICa1 via the input terminal CI is buffered via the buffer B1 before being fed to the next driving IC) ([0059]) (Fig. 4),
- (regarding claims 34, 40) the control units (14) of the functional unit control light source groups independently of a clock pulse that is predetermined by a line period provided for processing of a printed page (the timing control circuit 14 controls the corresponding light source group independent of a clock pulse governing the printing timing of the line image by controlling the lighting timing of the individual light emitting sections via the delay control circuit 18) ([0034]),

- (regarding claims 36, 42) the data comprise print data for the segments, corresponding to the light source group, of a plurality of lines to be printed (five data signals corresponding to five lines of image are stored at one time in the latch circuits 12a-12e as being fed from the shift register 11) ([0097]) (Fig. 4).

Response to Arguments

7. Applicant's arguments filed 02/26/08 have been fully considered but they are not persuasive.

Applicant argues that in Bizen, "[a] signal is sent out to all of the groups and then each group uses its own specific Y amendment data for the Y direction offset" and that "[n]o address decoder is provided in Bizen performing the functions of storing data in the memory as recited in claim 32". The examiner respectfully disagrees. Bizen teaches a central memory 5 for storing the Y direction amendment data, the appropriate amendment data being read out of the central memory 5 and written into the individual amendment data circuit internal to the corresponding driving IC (see paragraphs [0041], [0047]-[0048]). The reading and writing of data from and into a memory involves proper addressing of the locations within the memory circuit; In other words, the address decoder is an inherent part of the application. However, what Bizen fails to teach is the address decoder being integral to the functional unit. Regardless, Soma et al. teaches each of the driving ICs including an internal address decoder (21) for decoding an address signal (41) to output a signal indicative of the position of the respective light emitting diodes (30) in the array such that the lighting information signal can be received

by the proper light emitting diodes (Abstract). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the driving ICs of Bizen with the internal address decoders as taught by Soma et al. for the purpose of providing the driving circuitry with an efficient means for controlling and directing the correction data as well as the image data to the proper light emitting elements in the array to reduce the otherwise large external memory writing control.

Applicant further argues that "Bizen discloses at Figure 3 a clock input at timing control circuit 14 and data signals input at shift register 1" and that "there is no output via which the functional unit can forward data and a clock signal to the functional unit that is subsequent in the row except for the last functional unit in the row". The examiner respectfully disagrees. The examiner would like to draw the attention of Applicant to Bizen's Figure 2, which shows each driving IC having data input terminal SI and clock input terminal CI as well as the data output terminal SO and clock output terminal CO, such that the driving ICa26 can forward data and a clock signal to the driving ICa25 that is subsequent in the row, and the last driving ICa1 in the row having the data output terminal SO and clock output terminal CO left floating. Bizen further disclose in Figure 3 one of the driving IC in the row wherein the timing control circuit 14 having a clock input on the left side of the circuit and a clock output featured on the right side of the circuit, the clock output should be connected to the timing control circuit of the driving IC that is subsequent in the row, while the driving IC has also the data output terminals located on the right side of the driving IC.

Applicant also argues that neither Bizen not Katakura sow the functional units having a system clock by which the input signal is reproduced as recited in claim 33. The examiner respectfully disagrees. Bizen teaches the printer having a central control circuit 6 providing a clock signal to the clock input terminal CI of the driving ICa26, the clock signal being reproduced, e.g. forwarded, to the next driving ICa25 in the row, the clock signal being provided by an internal clock or system clock of the printer.

8. Applicant's arguments with respect to claims 32-45 have been considered but are moot in view of the new grounds of rejection.

Conclusion

9. Applicant's amendment, which changed the scope of the base claims, necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Luu can be reached on (571) 272-7663. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hai C Pham/
Primary Examiner, Art Unit 2861
May 17, 2008